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Electrical characteristics of β-Ga_2O_3 thin films grown by PEALD

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ABSTRACT

In this work, 7.5 nm Ga_2O_3 dielectric thin films have been deposited on *p*-type (1 1 1) silicon wafer using plasma enhanced atomic layer deposition (PEALD) technique. After the deposition, Ga_2O_3 thin films were annealed under N_2 ambient at 600, 700, and 800 °C to obtain β-phase. The structure and microstructure of the β-Ga_2O_3 thin films was carried out by using grazing-incidence X-ray diffraction (GIXRD). To show effect of annealing temperature on the microstructure of β-Ga_2O_3 thin films, average crystallite size was obtained from the full width at half maximum (FWHM) of Bragg lines using the Scherrer formula. It was found that crystallite size increased with increasing annealing temperature and changed from 0.8 nm to 9.1 nm with annealing. In order to perform electrical characterization on the deposited films, Al/β-Ga_2O_3/*p*-Si metal–oxide–semiconductor (MOS) type Schottky barrier diodes (SBDs) were fabricated using the β-Ga_2O_3 thin films were annealed at 800 °C. The main electrical parameters such as leakage current level, reverse breakdown voltage, series resistance (R_S), ideality factor (n), zero-bias barrier height (ϕ_{Bo}), and interface states (N_{SS}) were obtained from the current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements at room temperature. The R_S values were calculated by using Cheung methods. The energy density distribution profile of the interface states as a function of (E_{SS}–E_V) was obtained from the forward bias *I–V* measurements by taking bias dependence of ideality factor, effective barrier height (ϕ_e), and R_S into account. Also using the Norde function and *C–V* technique, ϕ_e values were calculated and cross-checked. Results show that β-Ga_2O_3 thin films deposited by PEALD technique at low temperatures can be used as oxide layer for MOS devices and electrical properties of these devices are influenced by some important parameters such as N_{SS}, R_S, and β-Ga_2O_3 oxide layer.

1. Introduction

Monoclinic Gallium oxide (β-Ga_2O_3) is one of the large band gap semiconductor materials and it has a direct band gap about 5 eV [1]. Since β-Ga_2O_3 features a higher dielectric constant (~10–14) than SiO_2 (~4) and has a unique transparency from the visible into the ultraviolet (UV) region, this material is very good candidate for industrial applications such as solar cells and optoelectronic devices operating at short wavelength, gate dielectric materials for complementary metal–oxide–semiconductor (CMOS) devices, next-generation high power devices, etc. [2,3]. In addition, metal/β-Ga_2O_3/semiconductor (MOS) type hydrogen sensor diodes with β-Ga_2O_3 reactive oxide films are very useful for hydrogen gas sensing since the reactive oxide intermediate layer between metal and semiconductor Schottky barrier diodes could improve the hydrogen gas sensing performance [4–6]. Ga_2O_3 has five crystalline modifications (α, β, γ, δ, ε) but β-form is the most stable crystalline modifications from room temperature to melting point of about 1800 °C. Also, β-Ga_2O_3 has a chemically stable even if it is exposed to concentrated acids such as hydrofluoric acid [7].

Because of these beneficial material properties, β-Ga_2O_3 thin films require the careful structural and electrical analysis. As known, growth techniques are crucial to obtain quality thin films. Variety of thin film deposition methods such as sol–gel method [8], metal–organic chemical vapour deposition (MOCVD) [9], sputtering, pulsed laser depositon [10], molecular beam epitaxy [11,12], and atomic layer deposition technique (ALD) [13–18] have been used to achieve better quality of β-Ga_2O_3 thin films. Unlike other physical vapor deposition (PVD) or chemical vapour deposition (CVD) methods, ALD is based on the saturative surface reactions, which results in a self-limiting growth mechanism. As a result, excellent conformality and large-area uniformity in addition to accurately controlled film thickness are inherently obtained. With the help of remote plasma, the processing temperatures can also be kept relatively low, which makes ALD attractive for a wide range of low-temperature compatible substrates including transparent and flexible polymers. At low deposition temperatures, to enable exchange reactions between the atoms or molecules, activation energy is required which might be provided via plasma activation

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Plasma-enhanced ALD (PEALD) technique is widely used as an alternative to conventional ALD. Thus, plasma source creates ions and radicals, enhance the chemical reactions and provide a wider range of materials which can be deposited at low temperatures.

In this study, we report on the growth of ~7.5 nm Ga_2O_3 thin films on *p*-type Si substrate using trimethylgallium (TMG) and O_2 plasma as the Ga source and oxidant, respectively and extraction of the main electrical parameters of Al/β-Ga_2O_3/*p*-Si (MOS) type SBDs using the *I–V* and *C–V* characteristics at room temperature. Also, annealing effect on the structural and microstructural properties of β-Ga_2O_3 thin films was discussed. To the best of our knowledge, such a study is not yet carried out on PEALD-grown β-Ga_2O_3 thin films.

2. Experimental method

Ga_2O_3 thin films were deposited by a Fiji F200 PEALD reactor (Ultratech/Cambridge Nanotech Inc.) using TMG as the Ga precursor and O_2 plasma as the oxidant with a base pressure of 0.20–0.25 Torr. Firstly, cleaning procedures were performed to *p*-type Si (1 1 1) wafers with 5 min sequential ultrasonic agitation in isopropanol, acetone, methanol, and de-ionized (DI) water. Afterwards, the wafers were treated in (1:19) HF: H_2O mixture for 1 min to remove native oxide on substrate surface. As the last step of the cleaning procedure, Si (1 1 1) wafer pieces were rinsed with DI water and dried by using N_2. After the cleaning procedure, wafers were loaded into the ALD reactor through a load lock. As mentioned in our previous group paper [18], in order to optimize growth parameters needed for the self-limiting deposition of Ga_2O_3 thin films, the effect of TMG dose, O_2 plasma duration, and Ar purge time were studied. Firstly, 500 cycles Ga_2O_3 films were deposited on a wafer to obtain thickness parameters with High Resolution Transmission Electron Microscope (HRTEM). After thickness calibration, 120 cycles were deposited at 250 °C, where one cycle consisted of 0.015 s TMG (precursor bottle temperature 6 °C)/5 s Ar purge/2–60 s (25 sccm, 300 W) O_2 plasma/5 s Ar purge. Postgrowth annealing of 120 cycles Ga_2O_3 films was performed in a rapid thermal annealing system (ATV-Unitem, RTP-1000–150) under 100 sccm N_2 flow at 600, 700, and 800 °C.

For structural characterization, HRTEM (FEI Tecnai G2 F30 transmission electron microscope) at an operating voltage of 300 kV was used for the imaging of Ga_2O_3 thin films. Also, to provide crystallographic information, Selected Area Electron Diffraction (SAED) measurement was carried out. Grazing-incidence X-ray diffraction (GIXRD) measurements were performed in a PANanalytical X'Pert PRO MRD diffractometer operating at 45 kV and 40 mA, using Cu K-α radiation. Initial scans were performed within the range of 10–90° by using 0.1° step size and 0.5 s counting time. For the crystalline samples, additional data were obtained within the same 2θ range by the summation of eight scans, which were performed by using 0.1° step size and 10 s counting time. Surface roughness and root-mean square (RMS) values were obtained by using Asylum Research, MFP-3D Atomic Force Microscope. In order to investigate electrical properties of β-Ga_2O_3 thin films, Al/β-Ga_2O_3/*p*-Si metal–oxide–semiconductor (MOS) type Schottky barrier diodes (SBDs) were fabricated using the β-Ga_2O_3 thin films which annealed at 800 °C with standard lithography process. All of the fabrication processes were conducted at class 100 and 1000 UNAM cleanroom facility. Back ohmic contact and top rectifier contact metallization was carried out by the thermal evaporation of a ~80 nm-thick aluminum (Al) layer using VAKSIS Thermal Evaporation system (PVD Vapor – 3S Thermal). Samples were annealed in ATV RTA system at 450 °C for 2 min under N_2 atmosphere for back-ohmic contact.

3. Results and discussion

For thickness controlling, firstly 500 cycles Ga_2O_3 film deposited on Si (1 1 1) at 250 °C and cross-sectional High Resolution Transmission Electron Microscope (HRTEM) image was carried out as in Fig. 1(a). Film thickness was measured as 26.7 nm from this image, which is in good agreement with the results obtained by ellipsometry.

Also, to provide crystallographic information, Selected Area Electron Diffraction (SAED) measurement was carried out and shown in Fig. 1(b). As can be seen from Fig. 1(b), as-deposited Ga_2O_3 film shows amorphous nature. In our sample, 120 cycles Ga_2O_3 film was deposited on Si (1 1 1) at 250 °C and thickness was also is in good agreement with ellipsometry measurements.

Fig. 2(a) and (b) show GIXRD patterns of as-deposited and annealed Ga_2O_3 thin films at different temperatures, respectively. As-deposited Ga_2O_3 thin films were found as amorphous structure. After annealing at 600 °C under N_2 atmosphere, β-phase Ga_2O_3 peaks began to appear and peak intensity increased and became sharper with increasing annealing temperatures. In Fig. 2(b), all of the main diffraction peaks in the GIXRD pattern can be indexed to a monoclinic β-Ga_2O_3 (ICDD reference code: 00–011-0370). This GIXRD pattern reveals that β-Ga_2O_3 has been synthesized successfully by using low-temperature PEALD and subsequent thermal annealing. In order to investigate the effect of annealing temperature on the microstructure of the Ga_2O_3 thin films, average crystallite size values were calculated according to Scherrer formula [19]

$$d = \frac{0.9\lambda}{\Delta\theta_B \cos\theta_B} \quad (1)$$

where, d is the average crystallite size, λ is the wavelength of the X-ray beam (0.15418 nm), $\Delta\theta_B$ is the full width at half maximum (FWHM) that was calculated from the XRD spectra, and θ_B is the Bragg angle.

As can be seen in Fig. 3, average crystallite size of the films was changed rapidly after annealing and increased with increasing annealing temperature. On the other hand, FWHM values for the most intense peak ($2\theta_B = 30.5$) is decreasing after annealing rapidly. The average crystallite size varied from 0.8 nm to 9.1 nm. This was evidence of improvement of crystal quality with increasing of annealing temperature. Also, 3D-AFM topographies were carried out to obtain idea about the surface morphologies and the root mean-square (RMS) values. 3D-AFM images were inserted in Fig. 2(a) and (b) for the as-deposited and annealed Ga_2O_3 thin films, respectively. RMS roughness values which was measured from 1 μm × 1 μm scan area were found as 0.16 and 0.37 nm for as-deposited and annealed thin films, respectively. It can be seen

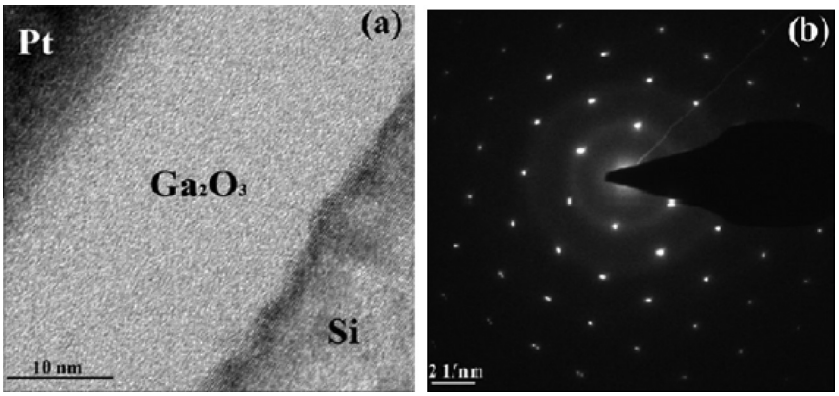

Fig. 1. (a) Cross-sectional HRTEM image of the Ga_2O_3 thin film deposited on Si (1 1 1) at 250 °C for thickness controlling. (b) SAED pattern of the same sample.

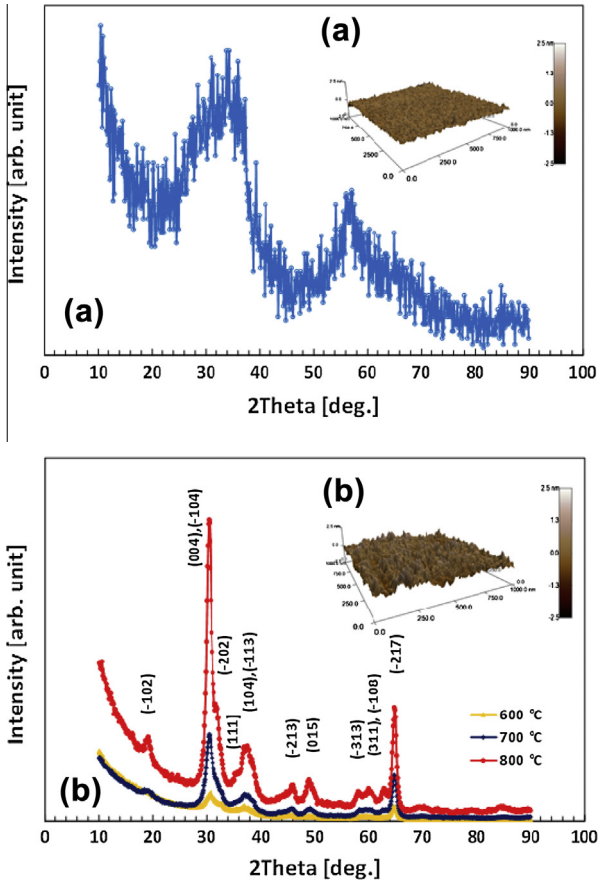

Fig. 2. (a) GIXRD patterns of as-deposited and (b) annealed Ga_2O_3 thin films. Also, 3D AFM images of as-deposited and annealed Ga_2O_3 thin films were inserted in (a) and (b), respectively.

that RMS roughness value increases after annealing. This situation was attributed to formation of grains upon crystallization.

To investigate electrical properties of Al/β-Ga_2O_3/*p*-Si SBDs, the *I*–*V* measurements were carried out at room temperature and are given in Fig. 4. As can be seen from Fig. 4, Al/β-Ga_2O_3/*p*-Si SBDs show good rectifying behavior.

Based on the thermionic emission model, *I*–*V* characteristics of a MOS type SBD under forward bias V (V>3kT/q) can be described by the following relationship [20]:

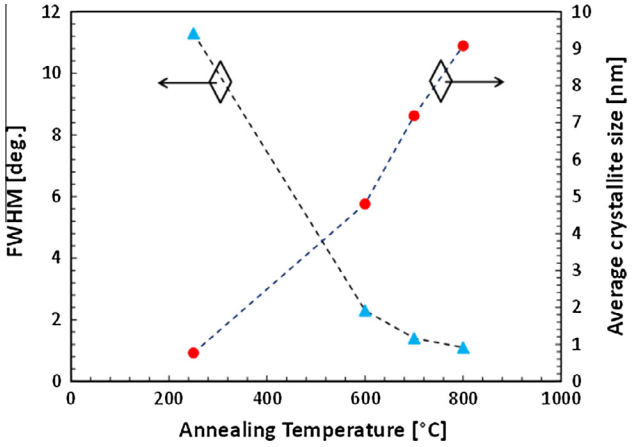

Fig. 3. The effect of annealing temperature on average crystallite size and FWHM (the most intense peak) values for PEALD grown Ga_2O_3 thin films.

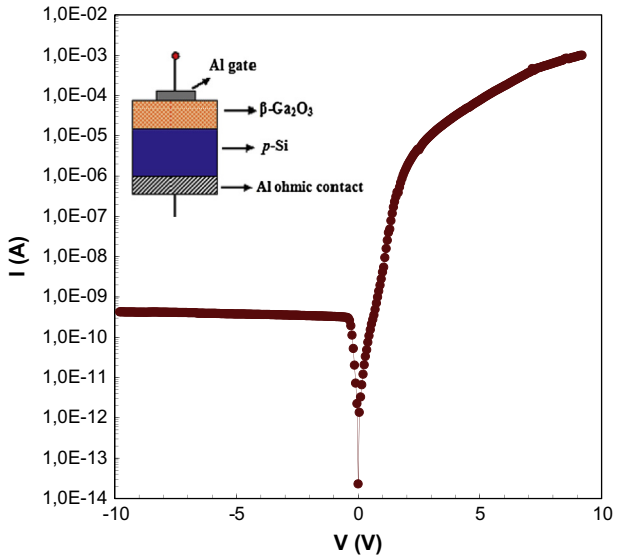

Fig. 4. The semi-logarithmic forward and reverse bias current–voltage characteristics of the Al/β-Ga_2O_3/*p*-Si (MOS) device at room temperature (inset figure shows structure of the device).

$$I_F = I_O\left[exp\frac{q}{nkT}(V - I_F R_S)\right] \tag{2}$$

where I_F is the forward current, V is the forward-bias voltage, R_S is the series resistance, q is the electronic charge, k is the Boltzmann constant, T is the temperature in K, n is the ideality factor, and I_o is the reverse bias saturation current and given by

$$I_O = AA^*T^2 exp\left(\frac{-q\phi_{Bo}}{kT}\right) \tag{3}$$

where A^* is the effective Richardson constant and equals to 32 A/cm^2 K^2 for *p*-type Si, ϕ_{Bo} is the zero-bias barrier height, A is the effective diode area and equals to 6.25×10^{-4} cm^2.

Using Eq. (2), the ideality factor is extracted from the slope of the linear region of the $ln(I_F$–$V)$ characteristics as

$$n = \frac{q}{kT}\left(\frac{d(V - I_F R_S)}{d(ln(I_F))}\right) \tag{4}$$

The value of zero-bias barrier height ϕ_{Bo} is determined from the intercepts of $ln(I_F)$ vs. V plot at room temperature. The experimental values of ϕ_{Bo} and ideality factors (n) were obtained as 0.95 eV and

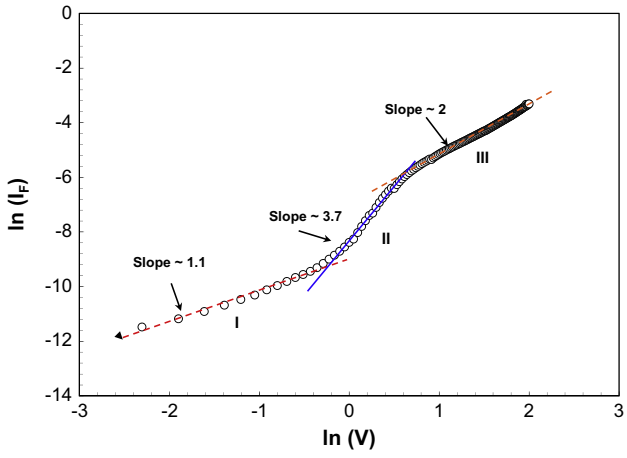

Fig. 5. ln(I_F) vs. ln (V) characteristics of Al/β-Ga_2O_3/*p*-Si SBDs at room temperature.

1.93 for Al/β-Ga_2O_3/*p*-Si SBDs, respectively. The *n* value is higher than unity. This situation is probably related to interface states and the effect of barrier inhomogeneities [21–23].

Also, I_F–*V* plot was drawn in logarithmic scale and is given in Fig. 5 to determine which current conduction mechanisms are dominant in the whole forward-bias region of the Al/β-Ga_2O_3/*p*-Si SBDs. Fig. 5 shows three linear regions with different slopes which are called region I, II, III. In these regions, I_F changes with V^m as proportional. Here, *m* is the slope of the $ln(I_F)$ vs. $ln(V)$ curve for each linear regions and were found as 1.1, 3.7, and 2 for the regions I, II, and III, respectively. In the region I (at low bias), I_F changes with $V^{1.1}$ and this indicates current conduction shows ohmic behaviour. In the region II (at middle bias), I_F changes with $V^{3.7}$ and this indicates current conduction shows power law voltage dependence and obeys the space-charge limited current (SCLC) theory. In the region III (at strong bias), the slope is 2 and this also indicates SCLC theory and in this region, because of strong carrier injection, the carriers escape from the traps and contribute to SCLC [22,24–27].

Also, the Norde method [28] was employed to compare effective barrier heights (ϕ_e) of the Al/β-Ga_2O_3/*p*-Si SBDs. The Norde function, *F*(*V*), being plotted against *V* as shown in Fig. 6. The *F*(*V*) function is defined as

$$F(V) = \frac{V}{2} - \frac{1}{\beta} ln\left[\frac{I_F(V)}{AA^*T^2}\right] \quad (5)$$

where $I_F(V)$ obtained from the I_F–*V* plot and β is a temperature dependent value calculated as $\beta = q/kT$. The $\phi_e^{(Norde)}$ is given by

$$\phi_e^{(Norde)} = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \quad (6)$$

where $F(V_{min})$ is the minimum point of *F*(*V*) curve and V_{min} is the corresponding voltage. From these equations, the $\phi_e^{(Norde)}$ value was calculated as 0.94 eV for Al/β-Ga_2O_3/*p*-Si SBDs and this value is good agreement with obtained from *I*–*V* method.

On the other hand, capacitance–voltage measurements (*C*–*V*) are normally used to calculate the ϕ_e value. Fig. 7 shows capacitance–voltage curve of Al/β-Ga_2O_3/*p*-Si SBDs at 1 MHz.

The linear plot of C^{-2}–*V* is very useful for analyzing the experimental *C*–*V* measurements and C^{-2}–*V* of MOS capacitor can be described by [20]

$$C^{-2} = \frac{2}{q\varepsilon_S A^2 N_A}(V_O + V) \quad (7)$$

where ε_S is the permittivity of the semiconductor (11.8), N_A the carrier doping density of acceptors, *V* magnitude of the revere bias, V_O is the intercept of C^{-2} with the voltage axis and is given by

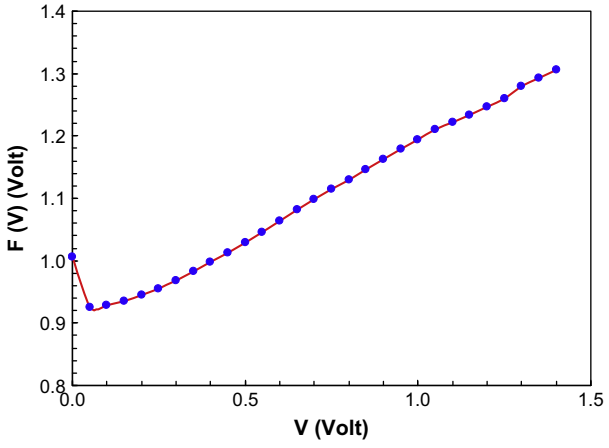

Fig. 6. *F*(*V*) versus *V* plot of the at Al/β-Ga_2O_3/*p*-Si SBDs at room temperature.

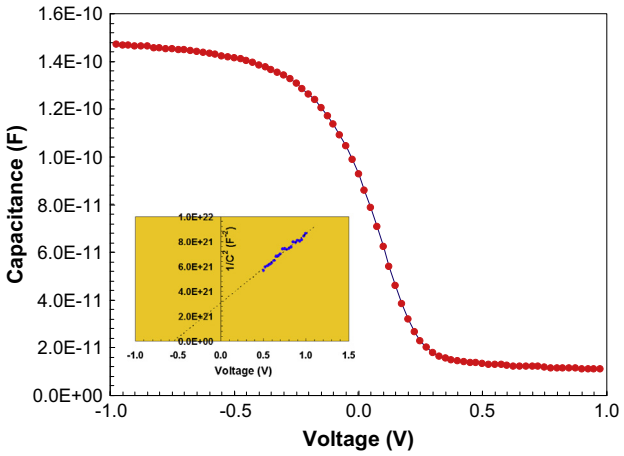

Fig. 7. High frequency *C*–*V* characteristic of Al/β-Ga_2O_3/*p*-Si SBDs (inset figure shows C^{-2}–*V* plot).

$$V_O = V_D - \frac{kT}{q} \quad (8)$$

The $\phi_e^{(C-V)}$ value can be obtained from

$$\phi_e^{(C-V)} = V_D + E_F - \Delta\phi_B \quad (9)$$

where E_F is the energy difference between the bulk Fermi level and valance band edge and can be calculated as

$$E_F = \frac{kT}{q} ln\left(\frac{N_V}{N_A}\right) \quad (10)$$

where N_V is the effective density of states in Si valance band. In Eq. (9), $\Delta\phi_B$ is the image force barrier lowering and is given by [29,30]

$$\Delta\phi_B = \left[\frac{qE_m}{4\pi\varepsilon_S\varepsilon_O}\right]^{1/2} \quad (11)$$

where E_m is the maximum electric field and given by

$$E_m = \left[\frac{2qN_A V_O}{\varepsilon_S\varepsilon_O}\right]^{1/2} \quad (12)$$

After extracting the values of V_o, E_F, and $\Delta\phi_B$, the values of barrier heights of $\phi_e^{(C-V)}$ can be calculated as

$$\phi_e^{(C-V)} = V_O + \frac{kT}{q} + \frac{kT}{q} ln\left(\frac{N_V}{N_A}\right) - \Delta\phi_B \quad (13)$$

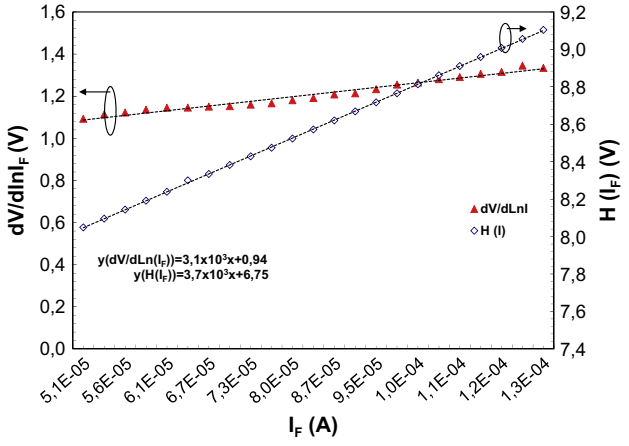

Fig. 8. Experimental dV/d(ln I_F) vs. I_F and (b) $H(I_F)$ vs. I_F plots for Al/β-Ga_2O_3/*p*-Si MOS device.

Table 1
The experimental values of main electrical parameters obtained from forward-bias *I–V* of Al/β-Ga_2O_3/*p*-Si SBDs at room temperature.

I_o (A)	n (*I–V*)	ϕ_{Bo} (eV) (*I–V*)	ϕ_e (eV) (Norde)	ϕ_e (eV) (*C–V*)	R_S (H(*I*)) (kΩ)	R_S (d*V*/dln(*I*)) (kΩ)	Reverse-breakdown field (MV/cm)
1.7×10^{-13}	1.93	0.95	0.94	0.95	3.7	3.1	50.7

From Eq. (13), $\phi_e^{(C-V)}$ was calculated as 0.95 eV. This value is in perfect agreement with the barrier height values determined via Norde and *I–V* method.

One of the important electrical parameters for this MOS type SBD device is the series resistance (R_S) because this parameter causes deviating from linearity of forward-bias *I–V* characteristics.

The voltage-dependent ideality factor $n(V)$ can be written from Eq. (2) as

$$n(V) = \frac{q}{kT}\left(\frac{d(V - I_F R_S)}{d(\ln(I_F/I_O))}\right) \tag{14}$$

R_S of the device is calculated from I_F–V measurement using a method developed by Cheung and Cheung [31] in the high-current range where the I_F–V characteristics are not linear due to series resistance. Cheung functions are given as

$$\frac{dV}{d\ln I_F} = n\frac{kT}{q} + I_F R_S \tag{15}$$

$$H(I_F) = V + n\frac{kT}{q}\ln\left(\frac{I_F}{AA^*T^2}\right) \tag{16}$$

and $H(I_F)$ is given as

$$H(I_F) = n\phi_{Bo} + I_F R_S \tag{17}$$

Eqs. (15) and (17) should give straight lines for the data of downward-curvature region in the forward-bias *I–V* characteristic. Fig. 8 shows these straight lines. Thus, the slopes of d*V*/d(ln I_F) vs. I_F and $H(I_F)$ vs. I_F graphs give R_S values.

The value of R_S calculated from the d*V*/d(ln I_F) vs. I_F plots of is closer to those obtained from the $H(I_F)$ vs. I_F plots and that indicates their consistency and validity. The obtained main electrical parameters are given at Table 1. It should be noted that there is a significant difference between the ideality factor obtained from the Cheung functions and *I–V* method. *I–V* method interests in the linear region of the *I–V* curve but Cheung method interests in the non-linear (downward) region. So, these differences can be sourced from some parameters such as series resistance, interface states, etc. because of these parameters are responsible with downward curvature of the *I–V* plot [32,33].

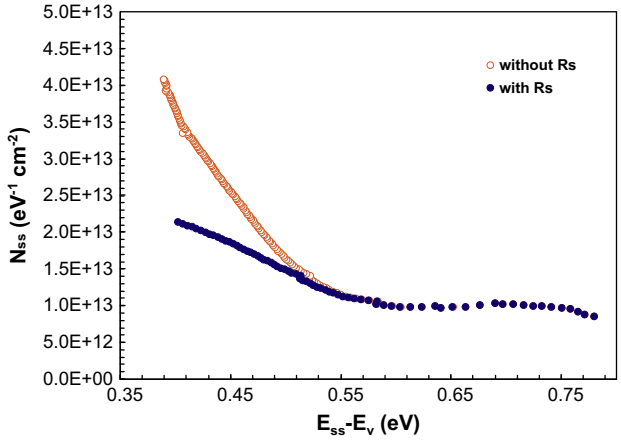

Fig. 9. The energy distribution profile of interface state densities obtained from the forward bias *I–V* characteristics of the Al/β-Ga_2O_3/*p*-Si SBDs.

The other important electrical parameter is interface states density that leads to the deviation of the ideality factor of SBDs at high current region. In general, for the oxide layer thickness larger than 3 nm, interface states communicate with the semiconductor. When an oxide layer and interface states occur, the applied bias voltage is shared by oxide layer, series resistance, and depletion layer of the device. The density of interface states can also be estimated from the current–voltage characteristics. In this case, the effective barrier height ϕ_e is used to place in the ϕ_{Bo} assumed to strongly dependent on electric field in the depletion region and applied bias due to presence of an interfacial insulator layer and interface states located between interfacial layer and semiconductor interface, and is given by [34,35],

$$\phi_e = \phi_{Bo} + \beta(V - IR_S) = \phi_{Bo} + (1 - 1/n)(V - IR_S) \tag{18}$$

where β is the changing coefficient of barrier height with bias. ϕ_e value includes the effects of both interface states in equilibrium with the semiconductor. Card and Rhoderick [36] proposed a formula to calculate interface states density as;

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_S}{W_D} + qN_{SS}(V)\right] \tag{19}$$

where W_D is the space charge width, N_{SS} is the density of interface states, ε_i is the permittivity of the interfacial layer, and δ is the thickness of the insulator layer. The values of δ and W_D were calculated from capacitance and conductance measurements (at 1 MHz) [20,37,38].

From Eq. (19), for a SBD having interface states in equilibrium with semiconductor, the interface state density N_{SS} can be obtained following equation

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \tag{20}$$

In addition, in *p*-type semiconductors, the energy of the interface states E_{SS} with respect to the top of the valence band at the surface of semiconductor is given by [39]

$$E_{SS} - E_V = q(\phi_e - V) \tag{21}$$

The obtained energy distribution profiles of N_{SS} are given Fig. 9. The interface-state density has an exponential rise with bias from the mid-gap toward the top of the valance band. As can be seen from Fig. 9, after series resistance corrections (taking into account R_S) is made, the interface states lowered. The magnitudes of the N_{SS} were found as without and with R_S corrections in 0.39-E_V are 4.2×10^{13} and 2.2×10^{13} $eV^{-1}cm^{-2}$, respectively. This situation shows clearly the effect of the series resistance and the series resistance value should be taken into account in determining the interface state density distribution curves. And finally, reverse-breakdown voltage of Al/β-Ga_2O_3/*p*-Si SBDs was measured as 38 V.

4. Conclusion

In this study, annealing effect on the structure and microstructure of PEALD grown β-Ga_2O_3 thin films was examined. Average crystallite size of the films was changed rapidly after annealing and increased with increasing annealing temperature. That means crystallinity of the films increased with increasing annealing temperature. Electrical characteristics of Al/β-Ga_2O_3/*p*-Si SBDs have been investigated by using *I–V* and *C–V* measurements at room

temperature using the β-Ga_2O_3 thin films as oxide layer which annealed at 800 °C. The main electrical parameters such as ideality factor (n), zero-bias barrier height (ϕ_{Bo}), leakage current level, series resistance (R_S), energy distribution profile of N_{SS}, and reverse breakdown voltage were obtained. The values of *Rs* were calculated using the Cheung methods. The energy distribution profile of N_{SS} was also obtained from the forward-bias *I–V* characteristics with and without series resistance corrections. All of the results suggest that β-Ga_2O_3 thin films, when subjected to annealing treatment following their deposition by PEALD at low temperatures using TMG as the Ga precursor and O_2 plasma as the oxidant, can be used for the fabrication of decent quality electrical devices.

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