Low temperature thin film transistors with hollow cathode plasma-assisted atomic layer deposition based GaN channels

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Low temperature thin film transistors with hollow cathode plasma-assisted atomic layer deposition based GaN channels

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We report GaN thin film transistors (TFT) with a thermal budget below 250 °C. GaN thin films are grown at 200 °C by hollow cathode plasma-assisted atomic layer deposition (HCPA-ALD). HCPA-ALD-based GaN thin films are found to have a polycrystalline wurtzite structure with an average crystallite size of 9.3 nm. TFTs with bottom gate configuration are fabricated with HCPA-ALD grown GaN channel layers. Fabricated TFTs exhibit n-type field effect characteristics. N-channel GaN TFTs demonstrated on-to-off ratios (I_{ON}/I_{OFF}) of 10^3 and sub-threshold swing of 3.3 V/decade. The entire TFT device fabrication process temperature is below 250 °C, which is the lowest process temperature reported for GaN based transistors, so far. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4884061]

GaN has earned an unrivaled popularity for high power applications and operation in harsh environments. GaN is a well-known, transparent semiconducting material with a band-gap of 3.4 eV. It is the material of choice in various applications such as high-electron-mobility transistors (HEMTs),[1] ultraviolet light emitting devices (UV LEDs),[2] chemical sensors,[3] UV photo detectors,[4] and power amplifiers.[5] Currently, there are mainly two deposition techniques most widely used for the utilization of epitaxial GaN films, namely, metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Both of these techniques offer single crystalline films; however, both necessitate high deposition temperatures.[6,7] In order to utilize GaN in settings with limited thermal budget, such as back end of line (BEOL) and flexible substrates, utilization of alternative deposition techniques carries vital importance. With this aim, low-temperature deposition of GaN has been reported, where different methods such as, sputtering,[8] pulsed laser deposition (PLD),[9] and atomic layer deposition (ALD)[10] were employed. Differing from other techniques, ALD offers the most uniform and conformal deposition even at sub-nanometer thickness levels.[11]

TFTs are the driving elements of the liquid crystal display technology.[12] Most commonly used active material in TFT-based technologies is amorphous Si (a-Si).[13] However, due to low carrier mobility in a-Si, high fabrication thermal budget, and strong absorption of visible light, a-Si is not suitable for flexible and transparent electronics applications. Therefore, a-Si has been challenged by several transparent metal oxides, of which the most famous one is ZnO.[14,15] TFTs with ZnO active layers have been reported to have electrical characteristics similar to or even better than those with a-Si.[16] However, stability problem of the ZnO TFTs still remains as an important issue. To overcome this problem by the use of an alternative material as the active layer of TFTs, Chen and colleagues[8] demonstrated devices with sputtered GaN channels, having a maximum process temperature of 1100 °C, which is prohibitively high for flexible electronics. Apart from their work, there are few other recent reports on the use of low-temperature deposited GaN in TFTs; however, all include high device processing temperatures, making them unsuitable for low temperature electronics.[17,18]

Here, we present hollow-cathode plasma-assisted atomic layer deposition (HCPA-ALD)-grown GaN based TFT with the lowest reported thermal budget so far, keeping the entire layer growth and device fabrication steps below 250 °C. Physical properties of GaN thin films and the electrical characteristics of the fabricated TFTs are discussed.

GaN thin films are deposited by HCPA-ALD, using trimethylgallium ($GaMe_3$) as the Ga precursor and N_2/H_2 gas mixture (50/50 sccm) with 300 W of plasma power as the N precursor at a process temperature of 200 °C. Grazing-incidence X-ray diffraction (GIXRD) measurements were carried out in a PANalytical X'Pert PRO MRD diffractometer using Cu K_α radiation, where the crystallite size of the thin film is calculated by the line profile analysis (LPA) method. Chemical composition of the GaN thin film is determined by X-ray photoelectron spectroscopy (XPS) using Thermo Scientific K-Alpha spectrometer with a monochromatized Al K_α X-ray source.

A 3-dimensional depiction of the proposed TFT is shown in Fig. 1(a), and a scanning electron microscope (SEM) image of the top view of the device is shown in Fig. 1(b). Fabrication of the bottom gate TFT starts with the RCA cleaning of the highly doped (1–5 mΩ-cm) p-type Si wafer. Plasma-enhanced chemical vapor deposition of a 200–nm-thick SiO_2 is performed at 250 °C. The SiO_2 film is patterned to define the active device areas. An HF-last clean is immediately followed by the growth of 77-nm-thick Al_2O_3 and 11-nm-thick GaN subsequently deposited at a single ALD process in a modified Fiji F200-LL ALD Reactor (Ultratech/Cambridge NanoTech Inc.), where the process temperature is kept at 200 °C. Active device areas are isolated by Ar-based dry etching of the GaN layer. Source and

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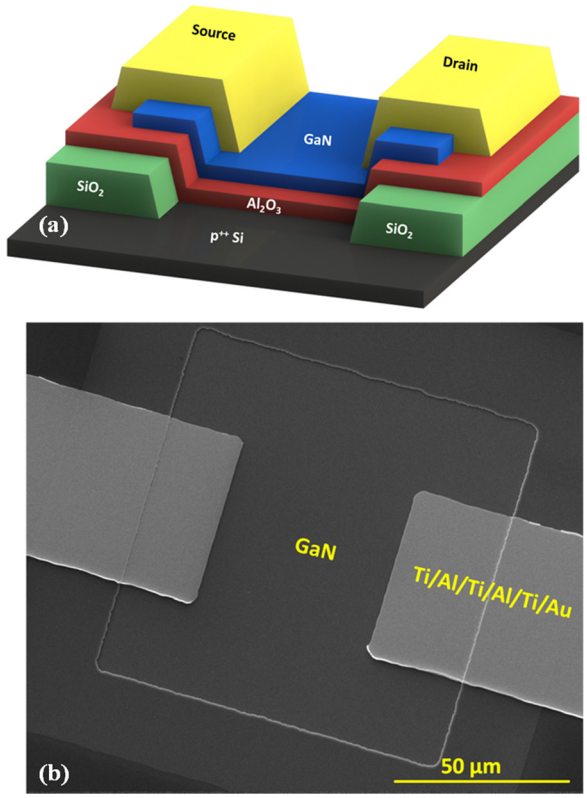

FIG. 1. (a) 3D schematic of the HCPA-ALD-based GaN TFT, (b) SEM image of the fabricated device.

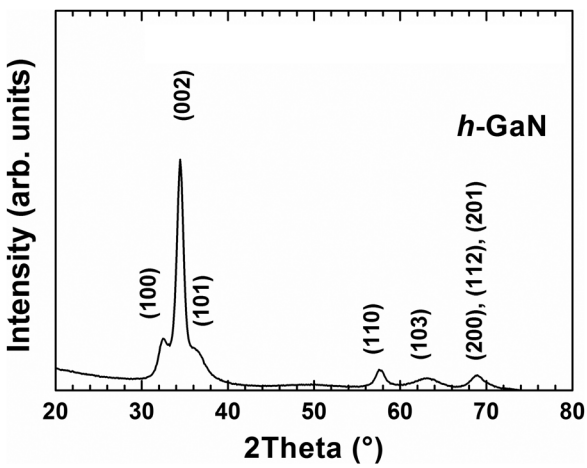

FIG. 2. GIXRD pattern of the HCPA-ALD-grown GaN thin film, which reveals a polycrystalline wurtzite crystal structure.

drain contacts are formed by sputtering a multilayer metal stack consisting of Ti/Al/Ti/Al/Ti/Au (30/30/30/30/30/60 nm) as suggested in Ref. 19. In order to keep the thermal budget of the device fabrication as low as possible, no annealing is applied after the contact metallization step. Fabricated TFTs have W/L = 1 with L = 50 μm. Electrical measurements of the devices are performed using Keithley 4200 semiconductor parameter analyzer.

The GIXRD pattern of the HCPA-ALD-grown GaN is shown in Fig. 2. Diffraction peaks obtained from the measurement, which correspond to wurtzite (hexagonal) crystal structure, reveal the polycrystalline nature of the deposited GaN thin film. The average crystallite size of the polycrystalline wurtzite GaN film is extracted from the (002) reflection and found to be 9.3 nm.[10] Chemical composition of the GaN thin film is obtained by making use of XPS with depth profile analysis, and 42.24 at. % Ga, 54.57 at. % N, 1.65 at. % O, and 1.54 at. % Ar are detected in the film after 60 s of Ar ion etching. Overestimation of the N content is observed due to the contribution of the Ga Auger peaks, which overlap with the N 1 s peak.[10]

Output electrical characteristics of the HCPA-ALD-based GaN TFTs are shown in Fig. 3(a). Fabricated devices have clear pinch-off and saturation characteristics, and they exhibit n-type field effect transistor behavior. Transfer characteristics of the devices with $V_{DS} = 1$ V applied are shown in Fig. 3(b). Fabricated TFT has an I_{ON}/I_{OFF} ratio of 2×10^3. The advantage of using a thick gate insulator is that the gate leakage current was kept below 0.5 pA for all the bias conditions. The threshold voltage of the device is extracted from the transfer characteristics (using $\sqrt{I_{DS}}$), and it is found to be 11.8 V. Sub-threshold swing (SS) of the device is generally influenced by trap states located in the forbidden gap. Extracted SS of the fabricated device is 3.3 V/decade. Charge mobility in the channel is extracted in the linear region of the device operation ($V_{GS} = 20$ V and $V_{DS} = 1$ V) by using the equation given in (1), where C_{ox} is the gate oxide capacitance per unit area. Relative permittivity of the ALD based Al_2O_3, required to calculate C_{ox}, is obtained from a previous study.[20] Calculated effective charge mobility in the channel is 0.025 cm^2/V-sec. This particularly low mobility can be attributed to the nanocrystalline structure of the HCPA-ALD based GaN thin films, and the surface states at the semiconductor insulator interface

$$\mu = \frac{I_{DS} \times L}{W \times C_{OX} \times \left((V_{GS} - V_{TH}) \times V_{DS} - \frac{V_{DS}^2}{2} \right)}. \quad (1)$$

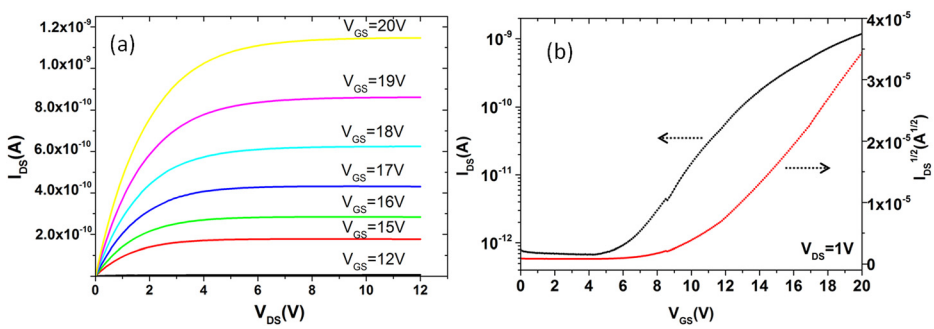

FIG. 3. (a) Output, and (b) transfer characteristics of the HCPA-ALD-based GaN TFTs.

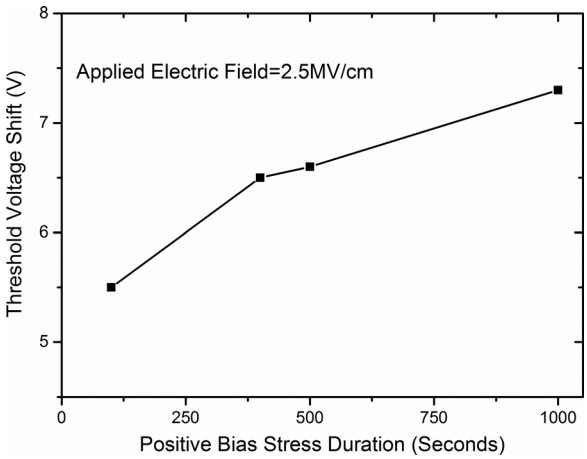

FIG. 4. Threshold shift vs. positive gate bias stress (2.5 MV/cm).

To further analyze the effect of trapped charges in the operation of the devices, effect of the positive gate bias stress on the threshold voltage is investigated, and the results are shown in Fig. 4. Prior to each stress cycle, devices are characterized by acquiring their transfer curves. A 2.5 MV/cm field is applied between the gate and source/drain of the TFTs while both drain and the source are kept at 0 V. Following the stress cycle, the transfer characteristics of the devices are obtained again. The difference in the threshold voltages between these measurements is recorded as the threshold voltage shift. Threshold voltage shift reveals the presence of charge trap states at the insulator semiconductor interface and or within the Al_2O_3 dielectric layer. As seen in Fig. 4, threshold voltage shifts to higher values with longer applied positive gate bias stress. This is due to increased number of trapped electrons which screen the applied gate field resulting in an increased threshold voltage. However, the increase in the threshold voltage after 1000 s of bias stress is smaller than that of high performance TFTs based on ZnO channels.[21]

In conclusion, GaN TFTs, with the lowest thermal budget to date, are fabricated with the utilization of HCPA-ALD method. Deposited GaN thin film is shown to have polycrystalline wurtzite structure with a crystallite size of 9.3 nm using GIXRD and LPA, respectively. Elemental analysis of the films revealed the low amount of oxygen in HCPA-ALD based GaN thin films. Output characteristics of the TFTs are obtained which show that the fabricated devices exhibit n-type enhancement mode field effect transistor behavior with clear pinch-off and saturation characteristics. Transfer characteristics of the devices show that the fabricated transistors have on-to-off ratios of 2×10^3. Finally, the effect of the positive gate bias stress on threshold voltage of the devices is studied, and reasonable threshold voltage shifts for a device with a considerably thick gate insulator are obtained. This study demonstrates the possibility of using low-temperature ALD-grown GaN layers for alternative and stable flexible/transparent TFT devices upon further materials and process optimization.

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